REMARKS

Applicants have carefully considered the June 30, 2005 Office Action, and the amendments above together with the comments that follow are presented in a bona fide effort to address all issues raised in that Action and thereby place this case in condition for allowance. Claims 1 and 4-23 are pending in this application. Claims 4-7 and 10-19 have been withdrawn from consideration pursuant to the provisions of 37 C.F.R. § 1.142(b).

In response to the Office Action dated June 30, 2005, claims 1, 20 and 23 have been amended. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the present Amendment should be apparent throughout the originally filed claims and the related discussion thereof in the written description of the specification. Applicants submit that the present Amendment places the application in condition for allowance and does not generate any new matter issue or any new issue requiring any further search and/or consideration. Accordingly, entry of the Amendment and prompt favorable reconsideration pursuant to 37 C.F.R. § 1.116 are respectfully requested.

Claims 1, 8, 9 and 20-23 were rejected under 35 U.S.C. § 102(b) as being anticipated over Terasawa (U.S. Pat. No. 6,002,143, hereinafter "Terasawa"). Applicants respectfully traverse the rejection for the reasons discussed *infra.*

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994). Moreover, in imposing the rejection under 35 U.S.C. § 102, the Examiner is required to specifically identify wherein an applied reference is perceived to identically disclose each feature of a claimed invention. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984). That burden has not been discharged. Moreover, there are significant differences between the claimed inventions and the device disclosed by Terasawa that would preclude the factual determination that Terasawa identically describes the claimed inventions within the meaning of 35 U.S.C. § 102.

Terasawa fails to disclosure or suggest a barrier-forming layer made of a second semiconductor having a bandgap-narrower than the first semiconductor, being in metallurgical contact with claimed reception layer so as to form a barrier for a tunneling injection of carriers at a heterojunction interface between the first and second semiconductors, as required in amended claim 1.

Terasawa fails to disclosure or suggest a method of fabricating a tunnel injection device comprising the steps of growing a layer made of a second semiconductor having a bandgap-narrower than the first semiconductor on a surface of the base body so as to form a heterojunction interface between the first and second semiconductors, as required in amended claim 20.

Terasawa fails to disclosure or suggest a means for forming a heterojunction interface so as to generate a band-edge discontinuity barrier for a tunneling injection of carriers at the heterojunction interface and means for supplying the carriers so as to accumulate the carriers at the heterojunction interface, being contacted with the source electrode, as required in amended claim 23.

Although the Examiner referred to Terasawa at FIG. 7, column 9 lines 50-67, and column 10 lines 1–9 as allegedly disclosing the present claimed subject matter, Terasawa admits that the basic structure of a MOS FET shown in FIG. 7 is identical to that of the MOS FET shown in FIG. 1 (See column 9, lines 54-56). At column 5, line 53 through column 6 line 18, Terasawa discloses that during the operation of the MOS FET, a bias voltage is applied across the drain electrode 18 and the source electrode 17 such that the drain is positive and the source is negative. Terasawa discloses that when no gate voltage is applied to the gate electrode 15, no inverted channel is formed at portions of the P^+ type silicon layer 13 which are brought into contact with the silicon oxide film 14, so that electrons supplied from the source electrode 17 are not conducted to the silicon carbide layer 12. Therefore, according to Terasawa, no current flows between the source electrode 17 and the drain electrode 18 and the semiconductor device is in an off- or non-conductive condition. When a positive voltage is applied to the gate electrode 15, negative charge is induced in portions of the silicon layer 13 adjoining the silicon oxide film 14 and an inverted channel is formed therein. Therefore, a current passes from the drain electrode 18 to the source electrode 17 via the silicon substrate 11, N^- silicon carbide layer 12, the inversion layer formed in the P^+ type silicon layer 13 and the source region 16. Furthermore, Terasawa, at column 9 lines 41-46, discloses that the inversion channel has to be formed within the silicon layer and silicon carbide layer. Terasawa discloses that if the inversion channel extends up to a boundary between the silicon substrate and the silicon carbide layer, a breakdown voltage might be reduced due to crystal incommensurate structure at the boundary.

Accordingly, in view of the foregoing, it should be evident that claimed tunnel-injection device (and the method of fabricating a tunnel-injection device) is operating with an absolutely different principle from the conventional MOS FET taught by Terasawa. In the claimed structure the current flowing between the source electrode and drain electrode is controlled by the tunneling probability penetrating through the energy barrier ΔEc formed at the heterojunction interface between claimed reception layer and the barrier-forming layer as shown in Figs. 2A to 2C. It is clear that, in Terasawa, the heterojunction interface formed between the P^+ type silicon layer 13 and the N^- silicon carbide layer 12 cannot function in such a way to control the tunneling injection current, which penetrates through the energy barrier ΔEc formed at the heterojunction interface between a reception layer and a barrier-forming layer. Terasawa merely provides a structure in which the N type diffusion layer 41 is formed in the surface region of the silicon carbide layer 12 adjoining the silicon substrate 11 so that the depletion layer formed at the P^+N^- junction cannot spread beyond the boundary between the bulk portion of the silicon carbide layer 12 and the N type diffusion layer 41. As a result, the depletion layer having a maximum electric field is formed within the same crystal without any crystal incommensurate structure, i.e. within the silicon carbide crystal (See column 9, line 66 to column 10, lines 9).

Therefore, it should be evident that there is no disclosure or suggestion in the applied art, of forming a barrier for a tunneling injection of carriers at a heterojunction interface between the first and second semiconductors (claims 1 and 20). Further, it should be evident that there is no disclosure or suggestion in the applied art of any means for forming a heterojunction interface so as to generate a band-edge discontinuity barrier for a tunneling injection of carriers at the heterojunction interface. As such Terasawa fails to identically disclose each limitation of the present independent claims and the rejection should be withdrawn for at least these reasons. The subject matter of dependent claims 8-9 and 21-22 is free from the applied art in view of their dependency from independent claim 1.

Furthermore, with respect to claims 1 and 20, Terasawa fails to disclose or suggest forming a gate electrode configured to change a tunneling probability of the carriers, which are configured to be injected into claimed reception layer by tunneling through the barrier, by controlling a width of the barrier. As evident from Terasawa's disclosure (column 5 line 53 through column 6 line 18 and column 9 lines 41-46) there is no disclosure or suggestion of a gate electrode configured to change a tunneling probability of the carriers, because the gate electrode of Terasawa is adapted for providing the inversion layer, or inverted channel at a surface of the P^+ type silicon layer 13, which are brought into contact with the silicon oxide film 14, in the conventional MOS FET.

Furthermore, Terasawa is silent regarding a drain region made of a first semiconductor, being contacted with a reception layer, configured to receive the carriers injected by tunneling through the barrier, as required in claim 1. It is evident that the region 11 contacted with the drain electrode 18 serves as the drain region, but the drain region 11 is made of N^+ silicon substrate in Terasawa (See column 5, lines 24-27, and column 8, lines 65-67).

The above argued differences between the present claimed subject matter and that of Terasawa's device undermine the factual determination that Terasawa discloses a device or method identically corresponding to that claimed. *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 230 U.S.P.Q. 86 (Fed. Cir. 1986). Applicants, therefore, submit that the imposed rejection of claims 1, 8, 9 and 20-23 under 35 U.S.C. § 102 for lack of novelty as evidenced by Terasawa is not factually viable and, hence, solicit withdrawal thereof.

It is believed that all pending claims are now in condition for allowance. Applicants therefore respectfully request an early and favorable reconsideration and allowance of this application. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, the Examiner is invited to call Applicants' representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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